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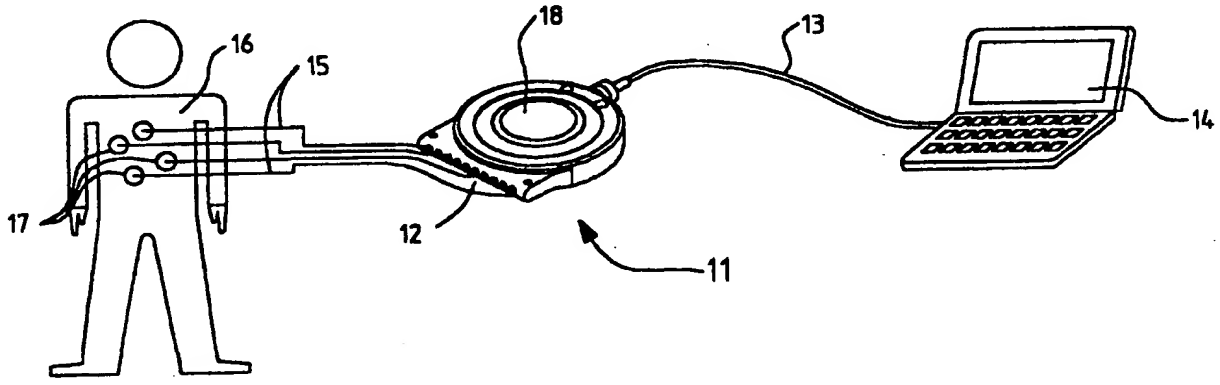

(57) Abstract

A universal ECG interface cable device (10, 40) comprising i. patient cable communication means (12, 112) adapted to connect to and be in electrical communication with ECG patient cables; ii. electrically isolated signal processing means (23, 123) adapted to preprocess ECG signals received by said patient cable communication means; iii. computer communication means adapted to receive preprocessed ECG signals from said signal processing means (23, 123) and transmit said preprocessed ECG signals to a universal communications port of a personal computer or like device. A cable formed from the cable device and a method of buffering and converting analog ECG signals to serial digital signals is also disclosed.

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UNIVERSAL ECG INTERFACE CABLE

The present invention relates to a universal ECG interface cable and, more particularly, to such a device adapted for acquisition of ECG signals from a patient and their communication to personal computers and like devices using standardised communication interfaces and protocols.

DISCUSSION OF PRIOR ART

The broad principles of the electronic acquisition of ECG waveforms, their electronic processing and subsequent display for interpretation of the condition of an in vivo heart have been known for some time.

Typically sufficient electrodes are applied to the body to obtain either single or multiple channel ECGs as the case may be and the raw signals are fed to a processing device. The electrodes can be directly attached to the processing device as, for example, described in the applicant's US patent US5123419 the specification of which is incorporated herein by cross reference. Alternatively the signals from the electrodes are conducted via cable to a separate, special purpose processing and display device which incorporates the necessary isolation to meet the electrical requirements of accepted electromedical safety standards such as, for example, IEC601.1 and the specific ECG standard IEC.601.2.25.

It is desirable to harness the power of the mass produced personal computer or like devices for at least the display and storage of ECG wave forms and the analysis thereof. To date, however, there has been a problem in providing the information to the personal computer or like

device in a simple convenient way. In addition it is desirable to maintain necessary electrical isolation as required by the aforementioned Standards. This can be a particular problem with high voltages applied during defibrillation to a patient which can damage electrical equipment (such as ECG devices) connected to the patient at the time.

It is an object of the present invention to ameliorate one or more of the abovementioned problems.

BRIEF DESCRIPTION OF THE INVENTION

In this specification the term "universal" as applied to the expression universal ECG interface cable denotes that the device can accept from a patient and transmit to a patient commonly accepted waveforms associated with ECG acquisition and can also communicate with computers and like data processing devices by means of a universal communications link, the universal link being, a common form of data communication means to the point it can be described as universal. Current computer communication links which would qualify as "universal links" include the RS232 serial link, the parallel port printer link and the IRDA infrared based serial link. The interface cable or device is thus "universal" in that it communicates to and from a patient in a manner as generally defined in the standards such as IEC601.2.5 and ANSI/AAMI EC 11-1991 and also communicates with personal computers and the like through industry standard and commonly available links and link protocols such as the universally recognised RS232C link.

It will thus be noted that embodiments of the device of the present invention necessarily require at least a cable for connection to a patient and a cable or link for connection/communication with a personal computer. Overall, therefore the device of the present invention takes the form of a "cable".

It will be observed from Fig. 1 that the cable of the present invention is relatively sophisticated and incorporates signal processing means which are housed in a bulbous portion of the cable. Hence, in this specification, the term "cable" is to be defined quite broadly so as to encompass housings for signal processing equipment and signal processing equipment which are in communication with conductors within the cable and which give the cable its ability to act as an interface device.

Embodiments of the present invention can be utilised as part of the patient data acquisition apparatus and/or the patient data transmission apparatus of the applicant's co-pending international application PCT/AU97/00821, the specification of which application is incorporated herein by way of cross-reference.

Accordingly, in one broad form of the invention there is provided a universal ECG interface cable device for a universal ECG interface cable comprising

i. patient cable communication means adapted to connect to and be in electrical communication with ECG patient cables;

ii. electrically isolated signal processing means adapted to preprocess the ECG signals received by said patient cable communication means;

iii. personal computer communication means adapted to receive preprocessed ECG signals from said signal processing means and transmit said preprocessed ECG signals in standard format to a universal communications port of a personal computer or like device.

Preferably said electrically isolated signal processing means comprises a microprocessor in communication with isolation means.

Preferably said isolation means includes means to receive and isolate a source of remotely communicated electrical power.

Preferably said source of electrical power comprises electrical power available from said universal communications port.

Preferably said source of power comprises a storage battery.

Preferably said universal communication port comprises one of a serial communications port; a parallel communications port or an IrDA infrared link port.

Preferably said microprocessor is in communication with memory means thereby to allow onboard storage within said interface device of ECG data, protocol data and analysis data and algorithms.

Preferably said protocol data includes error correcting hand shaking protocol data thereby to allow

error correction of data transmitted to said universal communications port from said interface device.

Preferably said source of electrical power is processed through a voltage regulator prior to processing by a voltage doubling circuit.

Preferably said signal processing means utilises a peak picking algorithm to compress digital data for transmission by said computer communication means.

Preferably said interface cable further includes buffering means comprising memory means adapted to store for a predeterminded period of time ECG waveform data prior to transmission via said personal computer communication means.

In a further broad form of the invention there is provided a method of converting analog ECG signals to digital signals for subsequent transmission via a universal port to a data processing device such as a personal computer; said method comprising utilising an ECG interface cable device comprising :

i. patient cable communication means adapted to connect to and be in electrical communication with ECG patient cables;

ii. electrically isolated signal processing means adapted to preprocess the ECG signals received by said patient cable communication means;

iii. personal computer communication means adapted to receive preprocessed ECG signals from said signal processing means and transmit said preprocessed ECG signals in standard format to a universal

communications port of a personal computer or like device.

Preferably said ECG interface cable device includes buffering means in the form of memory means adapted to store ECG data prior to transmission via said personal computer communication means.

Preferably said voltage regulator is selected to provide maximum power transfer at minimum expected input voltage from said source of electrical power.

Preferably said interface cable device further includes shunt means adapted to shunt large voltages experienced on said ECG patient cables.

In yet a further broad form of the invention there is provided a universal ECG interface cable comprising a universal ECG interface cable device as described above; said cable further including an ECG patient cable in communication with said patient cable communication means; said cable further including a link adapted to communicate at least ECG data between said personal computer communication means and said universal communications port of said personal computer or like device.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described with reference to the accompanying drawings wherein:

Fig. 1 is a perspective view of a universal ECG interface cable device according to a first embodiment of the invention,

Fig. 2 is a block diagram of the cable device of Fig. 1 connected to a portable personal computer,

Fig. 3 is a block diagram of the principles of isolation employed in the interface cable device of Fig. 1,

Fig. 4 is a block diagram of the main processing components in the interface cable device of Fig. 1,

Fig. 5 is an electrical schematic diagram of a typical ECG waveform pre-processing circuit, and

Fig. 6 illustrates a particular method of determining a "leads off" condition for the interface cable device of Fig. 1.

Fig. 7 is a schematic diagram of a specific implementation of the ECG interface device according to a second embodiment of the invention,

Fig. 8 illustrates body drive signal generation and sampling ticks as generated by the cable device of Fig. 7,

Fig. 9 lists commands for actuation of the cable device of Fig. 7 in tabular form.

Fig. 10 is a diagram of a "peak picking" compression algorithm utilised in the second embodiment of Fig. 7.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

1. First Embodiment

With reference to Fig. 1 there is shown a universal ECG interface cable device 10. It comprises a substantially circular in cross section case 11 having a series of ECG cable connectors 12 arrayed along an edge thereof and, in this example, a serial cable 13 extending from an edge surface diametrically opposed about case 11 from the connectors 12.

The interface cable device 10 is adapted to receive patient 16 ECG electrode cables connected at a first end to a patient and at the other end into the ECG cable connectors 12 on the case 11. The serial cable 13 is adapted for direct connection to a serial port on a personal computer (not shown in Fig. 1).

Fig. 2 illustrates the serial cable 13 connected to a portable personal computer 14 of the type adapted to rely on an internal power supply such as supplied by batteries. A number of patient cables 15 connecting from a patient 16 via electrodes 17 to the ECG cable connectors 12 connecting into the electronic acquisition unit 18 housed within case 11.

The electronic acquisition unit 18 includes isolation devices as illustrated in Fig. 3 adapted to provide electrical isolation between the RS232 signals 19 within serial cable 13 and the patient cables 15. In this instance the serial channel isolator 20 comprises opto isolators 21 for the data signals RXD and TXD. It further includes an isolated DC-DC converter circuit 22 incorporating an isolation transformer (not shown) for the power supply and other signals 19.

Fig. 4 is a block diagram of the main processing components within electronic acquisition unit 18 and shows serial channel isolator 20 communicating with microprocessor and A/D converter unit 23 which, in turn, communicates with patient cables 15 via amplifiers 24 and defibrillator protection device 25.

Typical amplifier circuits are illustrated in Fig. 5 and are available in the literature - see for example "Amplifiers for Bio-Electric Events: A Design with a Minimal Number of Parts" by A.C. Metting Van Rijn et al in Medical & Biological Engineering & Computing, May 1994 page. 305.

A triangle wave generator 26 superimposes a triangular wave on the driven leg drive circuit 27 for the purpose of communicating a "leads off" condition to microprocessor 23. The method of operation of this "leads off" facility will now be described in greater detail with reference to Fig. 6.

The standard technique for driving the right leg is used (see A.C. Metting Van Rijn) with addition of a 1000Hz triangle wave superimposed on the normal RLD signal. This triangle wave will appear as a common mode signal on all electrode inputs, and is of a sufficiently low level (10mV) to be of little concern if the electrodes are all well connected to the patient's body. Sampling of a particular lead is performed at identical times in the positive and negative halves of the triangle wave. When successive samples are averaged, the small residual common mode signal due to the generated triangle wave cancels out, resulting in a 2msec (500hZ) sampled system for each lead. When an electrode becomes disconnected, however, the small common mode signal due to this triangle wave becomes a very large unbalanced signal, and the difference between successive samples for a given lead will become very large. The difference between successive samples for a given lead will

therefore provide an indication of electrode contact quality, and an indication of leads off may be sent via the serial cable, to provide the appropriate operator warning.

With further reference to Fig. 4 the data processing and programmable capability of the universal ECG interface cable 10 derives primarily and importantly from inclusion of microprocessor 23 together with memory 28 within the electronic acquisition unit 18. This allows software routines to be included for communication with the serial port of a personal computer via serial cable 13 or with the IrDA transceiver 29 of a personal computer system whereby the universally provided communication facilities of a personal computer can be utilised, thereby obviating the need for special purpose interconnections to the personal computer or the inclusion of separate processing cards connected to the bus of the personal computer. The ECG waveform information derived from patient connection 15 and preprocessed by microprocessor 23 is thereby directly available in standard form to the microprocessor comprising the personal computer without any further preprocessing steps requiring non-standard or non-conventional hardware in the personal computer or like device.

The ECG interface cable device 10 provides diagnostic quality multi-lead ECG in digital serial RS/232 compatible form to meet all aspects of both AAMI EC11 and IEC601 (IEC601.1 and IEC601.2.25 (class BF or CF)). It is intended to be compact, inexpensive and capable of transmitting diagnostic quality ECG via a standard serial lead (RS232) or standard infrared link (IrDA) to any

general computer and associated software. Note that the ECG standards include both conventional 12-lead ECG systems and more specialised lead sets used in vectorcardiography.

The unit consists of multiple patient cables (for connection to a person's body) entering a compact enclosure, containing electronics that processes and digitises the ECG signals, converting the data to serial form for transmission down a separate cable that connects to a computer's serial port. Figure 1 shows an enclosure for a 10 patient electrode, standard 12-lead ECG system.

The use of active electronics in the acquisition unit 18 facilitates the reduction of electrical noise via the use of short patient cables.

The serial communication is bidirectional for flexibility and electrically isolated for patient and operator safety. Alternatively, communication can be by the naturally isolated, wireless IrDA method of serial data communication. Power for the device may be derived either by battery, or via an isolation transformer in the serial cable. The latter technique, in particular, requires extremely low power consumption in the system electronics.

2. Second Embodiment

Like components are numbered as for the first embodiment, except with the prefix 1. So, for example, microprocessor 23 becomes microprocessor 123 in the second embodiment. In this instance, with reference to Fig. 7, the major components are ECG cable connectors 112 connecting to amplifiers 124 which feed to microprocessor and analog to digital converter 123. Serial output from

the microprocessor and analog digital converter assembly 123 to serial cable 113 is buffered by serial channel isolator 120. The DC to DC converter circuit 122 derives power from the DTR and RTS lines of serial cable 113.

DTR and RTS are shorted together to minimise serial impedance which would decrease efficiency. They can vary 5.5V - 10V (no load voltage). The major problems would be expected at the low end of the range.

So, in this embodiment, a minimum no load input voltage is expected to be about 6V. The voltage regulator is selected so that maximum output power with a load would occur when the load brings the output voltage to about 3V. The MAX8863SEUK-T is a 2.84V ultra low dropout regulator. With the isolation transformer shown, VCC will be regulated to about 3.5V.ISOVCC is a doubled version of the 2.84V supply ie. 5.5V (with diode drop). This supplies the CMOS inverter that drives RXD. ie. RXD is 0 or 5.5V, which is compatible with virtually all RS232 inputs.

The optiosolators are configured as normally OFF to save power when not transmitting.

High voltage isolation from, for example, defibrillation, is provided by shunt circuit 42 in Fig. 7, which circuit comprises input resistor R1, shunt device comprising gas discharge tube G1 and second voltage drop resistor R2. This circuit acts to prevent high voltages such as those arising during defibrillation from reaching amplifiers 124.

In this instance R1 is a 10K solid carbon composition resistor 0.5Wats; R2 is a standard 0.125W carbon film

resistor and G1 is a gas discharge tube which arcs at approximately 100 volts.

Resistor R1 should be a solid carbon composition resistor because of the relatively large peak currents of approximately 0.5amp. This arrangement minimises the possibility of fusing of resistor R1. Expected peak current in resistor R2 should only be about 10mA, hence it may be of carbon or metal film construction.

A schematic diagram of a device 40 according to a second embodiment is shown in Fig. 7. The device 40 connects to a person via the 10 electrode cables: LL, LA, RA, RL, V1, V2, V3, V4, V5, V6. ECG information is to be sent via a serial cable 113 to either a specialised device such as described in US5123419 or as currently marketed by the applicant under the trade mark BIOLOG or a general purpose computing device loaded with an appropriate program for processing the serial data and displaying the ECG waveforms and related data.

The relevant functional standards may be found in standard ANSI/AAMIEC11-1991.

Where data buffering is required in order to match data flow to the speed of the capacity of the serial cable 113, additional memory can be connected to the microprocessor and analog to digital converter assembly 123.

As can be seen from figure 7 all leads are referenced to the left leg electrode. A right leg drive circuit is also included.

2.1 Lead Derivations

let LA' = LA-LL,

RA' = RA-LL,

Vi' = Vi - LL, for 1 an integer from 1 to 6 inclusive. Leads marked with a ' are relative to the left leg electrode.

The standard 12 leads are given by:

I = LA-RA = **LA'-RA'**

II = LL-RA = **-RA'**

III = LL-LA = **-LA'**

WCT = 1/3* (LL + RA +LA)

WCT' = 1/3* (RA' + LA')

aVR = 1.5** (RA-WCT) = **1.5* (RA' - WCT')**

aVL = 1.5** (LA - WCT) = **1.5* (LA' - WCT')**

aVF = LL - 0.5* (LA + RA)

= 0.5* (2* LL-LL-LA-RA)

= **-0.5* (LA' + RA')**

lead V1 = V1 - 1/3* (LL + RA + LA)

= **V1' - WCT'**

similarly,

lead V2 = **V2' - WCT'**

lead V3 = **V3' - WCT'**

lead V4 = **V4' - WCT'**

lead V5 = **V5' - WCT'**

lead V6 = **V6' - WCT'**

Notice that all of the standard twelve leads may be derived directly from the eight measured values, RA-LL, LA-LL, V1-LL, V2-LL, V3-LL, V4-LL, V5-LL and V6-LL. The device will therefore transmit leads, I, II, and V1 - V6. All other leads may be derived from these values.

2.2 Shield Drive Circuit

The shield drive has been disconnected in this version to prevent instability. The shield is connected to analog ground instead.

2.3 Right Leg Drive Circuit

This is based on that designed by Metting Van Rijn, with the exception of a common mode body drive signal. This signal is to be used for leads off detection. It works in the following manner (refer to the figure 7 circuit diagram and to Fig. 6).

Amplifier U1A works as a conventional integrator of the body reference signal, derived from the LL signal. In fact, the circuit should behave as a conventional RL drive circuit with U1B removed.

If the processor toggles pin 36 at 1000Hz U1A will integrate this square wave into a triangle wave, and drive the body with it. Note that as the body forms part of a negative feedback loop, the integrator U1A will attempt to reduce this triangular signal to zero. To prevent this from occurring, it is necessary to also subtract a similar triangular wave from the body reference signal. This is done by U1B (an integrator similar to U1A). The amplitude of the triangle wave applied to the body is set to about 6mV p-p.

This triangle wave appears as a common mode signal on all electrodes. if the electrodes are correctly placed on the body, the input amplifiers will amplify the signal by their common mode voltage gain (~1). Thus each input signal will contain a small amount of residual 500Hz ripple

in normal operation. If an electrode becomes detached, the 500Hz body drive signal is no longer a common mode signal and will be amplified by the huge differential gain of the stage. This is easy to detect on any lead.

Note that the 1000 Hz ECG sampling is synchronous with the normal 500Hz ripple, so it should be possible to remove this interference from the ECG data. If two successive samples are added, the positive and negative offsets from zero will be equal, so will cancel each other. If these offsets are beyond a certain threshold the lead can considered to be off. The resulting sampling rate will be 500Hz. The amplitude of the sawtooth should be selected to be an absolute minimum to enable reliable leads on/off detection. See figure 6:

A 1000Hz sampling interrupt must be established in the processor. Pin 36 is toggled every tick. All leads are sampled every tick. The amplitude of the sawtooth may be calculated for each lead. If the sawtooth amplitude deviates significantly from the average (gets larger) the electrode contact will be poor and leads off can be signalled for that lead.

3. Software Operation

The device will basically have two modes: command mode and acquisition mode. The default mode on reset is command mode. In this state the device is waiting for instructions from the serial port. The data rate on the serial port is 115,200 baud (n, 8, 1). Any unknown character string received before a carriage return will cause the processor to issue the response **ERROR - what?**

Twenty communications errors (non-ASC11 characters or framing errors) will also cause the same response.

3.1 Command Mode

Command mode is the default mode for the device. It is used to:

- establish communications
- query and identify the device
- change the configuration or operation of the device.

Commands and responses are generally in simple ASC11 text, unless stated otherwise. They are terminated by the <CR> character. Command characters are echoed by the device, and a response is required to all commands. Commands may be followed by parameter(s) (separated by spaces), also in ASC11.

The standard acknowledge signal is OK. Any other invalid response should be considered as an error. When a valid response other than OK is returned, multiple items are separated by semicolons. All responses are terminated by <CR>.

A list of commands and parameters (from the computer 114) and response (from the device 40) are shown in Fig. 9. In this case, a simple terminal emulation program known as TELIX is utilised both as a development aid and debug tool. This enables code development without the need for writing specialised software on the other end.

Command mode is entered either from power up or from an aborted data transmission (one or more CAN characters received during a transmission).

3.2 Data Transfer Mode

Data transfer mode is entered by issuing the **data** command. A predetermined protocol is used for the data transfer, which can be based on known protocols such as Xmodem. Note that commands are not accepted during ecg acquisition mode.

3.4 Data Transfer Implementation

Terminology

A suitable command sequence is shown below (speed 115,200 baud). <CR> after each command and response not shown.

COMPUTER	INTERFACE DEVICE
enq	→
	← OK
id	→
	← BIOSYNCH12;hwV1.1;swV1.3
res	→
	←2971;12
ecg 1	→
	← OK
data	→
	← OK
	← single lead data

Note: if the computer 114 sends one or more CAN characters (CTRL-X), transmission will be aborted and device 40 will revert to COMMAND mode.

ecg all	→
	← OK
data	→
	← OK
	← 12 lead data

Overview

The leads to be transmitted in acquisition mode are first defined by the **ecg** command.

Transmission does not commence until the **data** command is received by the transmitting device. It responds with **OK**, then starts sending data.

ECG Single Lead Data Structure

There are two kinds of data.

The first is for sending data from single **standard** leads (ie. one of I,II,III,aVR,aVL,AVF,V1,V2,V3,V4,V5,V6).

Every sample period (2 msec), one sample is sent over the serial line. This consists of 2 bytes, separated by about a 15msec gap to help prevent data overrun. Data is sent most significant byte first, in unsigned format.

First byte:

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	D11	D10	D9	D8	D7	D6	D5

Second byte:

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	D4	D3	D2	D1	D0	S1	S0

Bit 7 is used as an aid to synchronise the data.

D11...D0 represent the 12 bits of the lead data

S1 and S0 are special bits

S1	S0	Meaning
0	0	normal data
0	1	leads off detected
1	0	data is saturating amps and leads are being zeroed

1 1 pacing detected (must be enabled by **pacing on** command).

12 Lead Data Structure

If all 12 leads are requested (**via ecg all**), the 8 standard leads are transmitted in 2 blocks, at 1 msec intervals, as follows.

Block1

byte 1 most significant 8 bits of lead 1

byte 2 least significant 4 bits of lead 1, Most significant 4 bits of lead 11

byte 3 least significant 8 bits of lead 11

byte 4 most significant 8 bits of lead V1

byte 5 least significant 4 bits of lead V1, Most significant 4 bits of lead V2

byte 6 least significant 8 bits of lead V2

Block2 (1 msec from commencement of block 1)

byte 7 most significant 8 bits of lead V3

byte 8 least significant 4 bits of lead V3, Most significant 4 bits of lead V4

byte 9 least significant 8 bits of lead V4

byte 10 least significant 8 bits of lead V4

byte 11 least significant 4 bits of lead V5, Most significant 4 bits of lead V6

byte 12 least significant 8 bits of lead V6

byte 13 linear 8 bit unsigned checksum of bytes 1..12 inclusive

Again data is in unsigned, standard format.

This entire structure is sent at 2msec intervals, to provide 500Hz sampling.

Data for each lead is limited to OxFEF. Values of OxFFO and above are reserved. The following values have meaning at present.

OxFFO - lead is being zeroed

OxFF1 - lead is off

OxFF2 - pacing spike detected (pacing must be ON).

Typical serial data speeds for serial links which would fall within the definition of "universal" as used in this specification typically can reach speeds (with present technology) of only up to about 115200 baud. This presents a problem where 500Hz sampling is used because this sample rate is not sufficient to pass the EC11 20msec triangle wave test (test no. 3.2.7.2 method D). Sampling at 1000Hz will pass the test but, in the embodiment described above, this amount of data cannot be sent in real time at 115200 baud. That is, 8 channels of 1000Hz 12 bit data cannot be sent in real time at 115200 baud.

In this embodiment sampling is performed at 1000Hz with " peak picking" to be used as a compression algorithm to form 500Hz sampled data for transmission over the serial link. The peak picking algorithm is shown diagrammatically in Fig. 10. The algorithm looks at two consecutive sample points and selects that sample point of the two which is the furthest as compared with the last selected data point for transmission.

In use the interface device 10, 40 of either of the first or second embodiment is connected to an ECG cable 12,

112 which, in turn, is connected by electrodes to a patient whose ECG is to be measured. A serial cable 13, 113 is connected from the interface device 10, 40 to a personal computer 14, 114. The personal computer includes a program (for example as described in the applicant's co-pending international application PCT/AU97/00821 referenced earlier) which is adapted to receive the digitised data stream from the interface cable device and store and/or display the data in a meaningful way for those skilled in the art to interpret the ECG data.

The above describes only some embodiments of the present invention and modifications, obvious to those skilled in the art can be made thereto without departing from the scope and spirit of the present invention.

For example other numbers of leads can be used for connecting to the patient. In particular simplified forms of ECG acquisition can utilise a lesser number of conductors between the patient and the case.

Whilst particular embodiments have been described utilising an RS232 serial interface, other universal communication interfaces can be utilised such as IRDA.

INDUSTRIAL APPLICABILITY

The present invention particularly applicable to facilitate the connection of patient ECG electrodes to a data processing device in a convenient manner whilst still adhering to all the necessary standards.

CLAIMS

1. A universal ECG interface cable device for a universal ECG interface cable; said device comprising

i. patient cable communication means adapted to connect to and be in electrical communication with ECG patient cables;

ii. electrically isolated signal processing means adapted to preprocess the ECG signals received by said patient cable communication means;

iii. personal computer communication means adapted to receive preprocessed ECG signals from said signal processing means and transmit said preprocessed ECG signals in standard format to a universal communications port of a personal computer or like device.

2. The interface cable device of Claim 1 wherein said electrically isolated signal processing means comprises a microprocessor in communication with isolation means.

3. The interface cable device of Claim 2 wherein said isolation means includes means to receive and isolate a source of remotely communicated electrical power.

4. The interface cable device of Claim 3 wherein said source of electrical power comprises electrical power available from said universal communications port.

5. The interface cable device of Claim 3 wherein said source of power comprises a storage battery.

6. The interface cable device of any previous claim wherein said universal communication port comprises one of

a serial communications port; a parallel communications port or an IrDA infrared link port.

7. The interface cable device of any one of Claims 2-6 wherein said microprocessor is in communication with memory means thereby to allow onboard storage within said interface device of ECG data, protocol data and analysis data and algorithms.

8. The interface cable device of Claim 7 wherein said protocol data includes error correcting hand shaking protocol data thereby to allow error correction of data transmitted to said universal communications port from said interface device.

9. The interface cable device of claim 4 wherein said source of electrical power is processed through a voltage regulator prior to processing by a voltage doubling circuit.

10. The cable device of any previous claim wherein said signal processing means utilises a peak picking algorithm to compress digital data for transmission by said computer communication means.

11. The interface cable device of any previous claim further including buffering means comprising memory means adapted to store for a predeterminded period of time ECG waveform data prior to transmission via said personal computer communication means.

12. A method of converting analog ECG signals to digital signals for subsequent transmission via a universal port to a data processing device such as a personal computer; said

method comprising utilising an ECG interface cable device comprising:

i. patient cable communication means adapted to connect to and be in electrical communication with ECG patient cables;

ii. electrically isolated signal processing means adapted to preprocess the ECG signals received by said patient cable communication means;

iii. personal computer communication means adapted to receive preprocessed ECG signals from said signal processing means and transmit said preprocessed ECG signals in standard format to a universal communications port of a personal computer or like device.

13. The method cable of Claim 12 wherein said electrically isolated signal processing means comprises a microprocessor in communication with isolation means.

14. The method of Claim 13 wherein said isolation means includes means to receive and isolate a source of remotely communicated electrical power.

15. The method of Claim 14 wherein said source of electrical power comprises electrical power available from said universal communications port.

16. The method of Claim 15 wherein said source of power comprises a storage battery.

17. The method of any one of claims 12 to 16 previous claim wherein said universal communication port comprises one of a serial communications port; a parallel communications port or an IrDA infrared link port.

18. The method of any one of Claims 12 to 16 wherein said microprocessor is in communication with memory means thereby to allow onboard storage within said interface device of ECG data, protocol data and analysis data and algorithms.

19. The method of Claim 18 wherein said protocol data includes error correcting hand shaking protocol data thereby to allow error correction of data transmitted to said universal communications port from said interface device.

20. The method of claim 15 wherein said source of electrical power is processed through voltage regulator prior to processing by a voltage doubling circuit.

21. The method of any one of claims 12 to 20 wherein said signal processing means utilises a peak picking algorithm to compress digital data for transmission by said computer communication means.

22. The method of any one of claims 12 to 21 wherein said ECG interface cable includes buffering means in the form of memory means adapted to store ECG data prior to transmission via said personal computer communication means.

23. The method of claim 20 wherein said voltage regulator is selected to provide maximum power transfer at minimum expected input voltage from said source of electrical power.

24. The method of any one of claims 12 to 23 further including shunt means adapted to shunt large voltages experienced on said ECG patient cables.

25. A universal ECG interface cable comprising a universal ECG interface cable device as claimed in any one of claims 1 to 11; said cable further including an ECG patient cable in communication with said patient cable communication means; said cable further including a link adapted to communicate at least ECG data between said personal computer communication means and said universal communications port of said personal computer or like device.

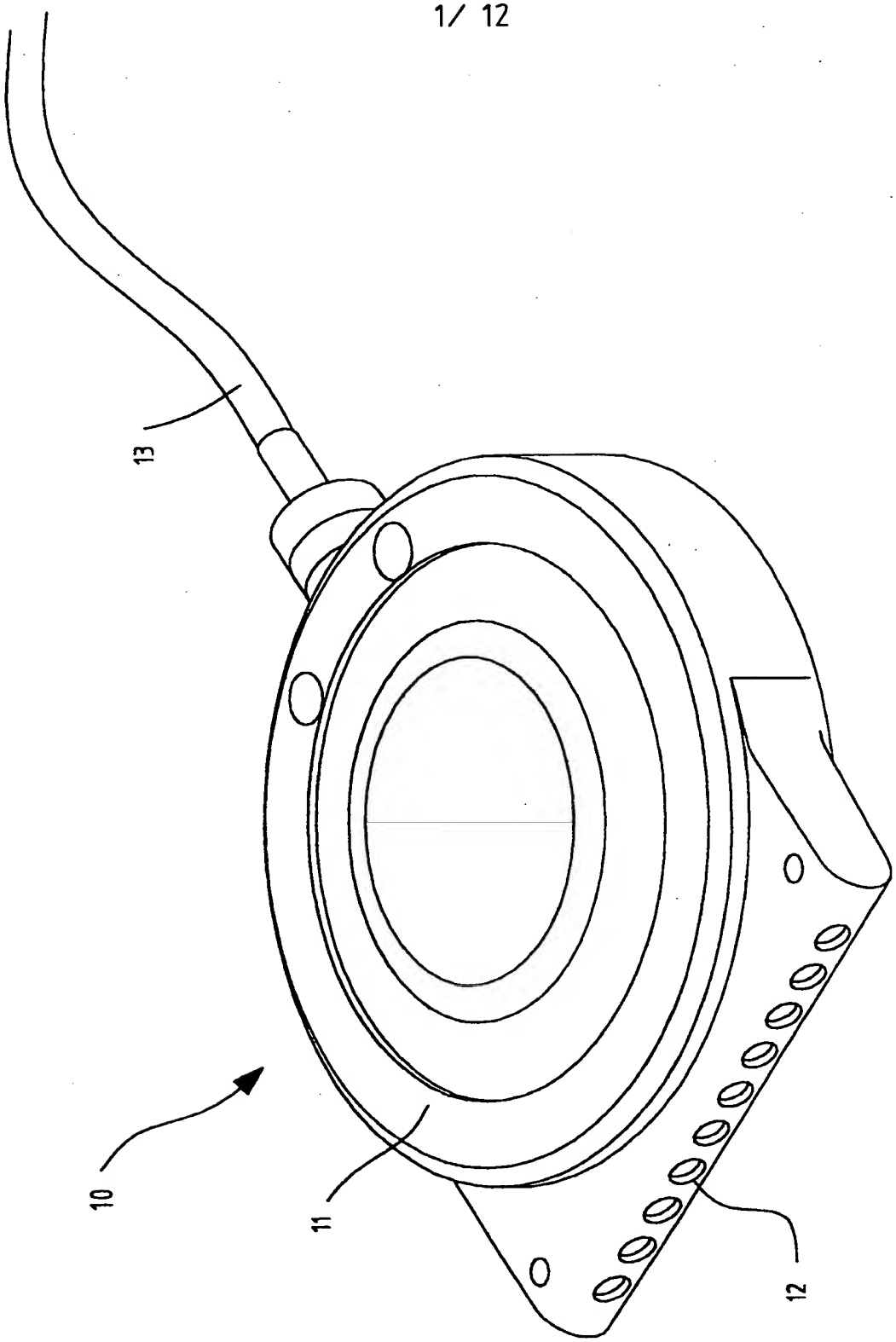


Fig. 1

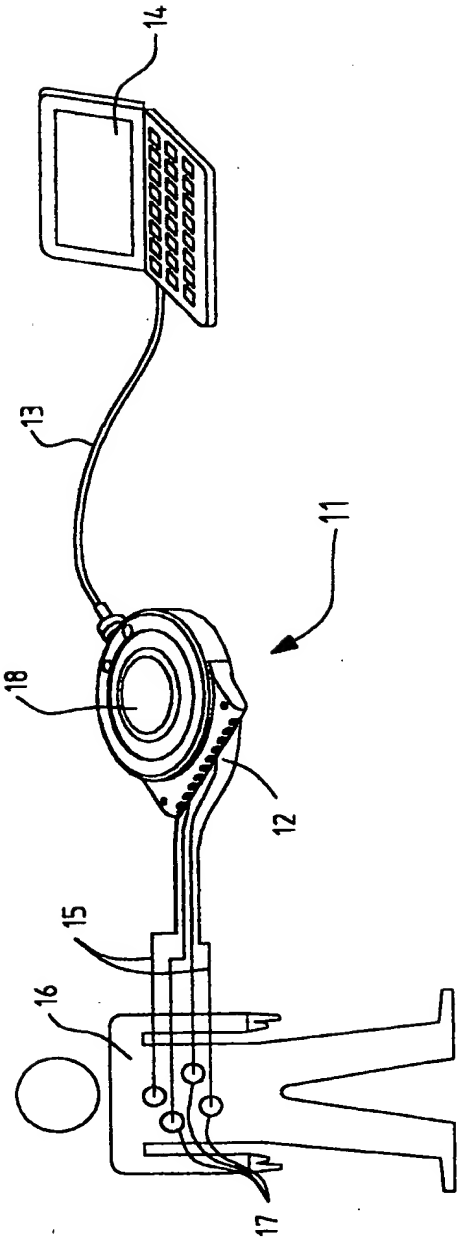


Fig. 2

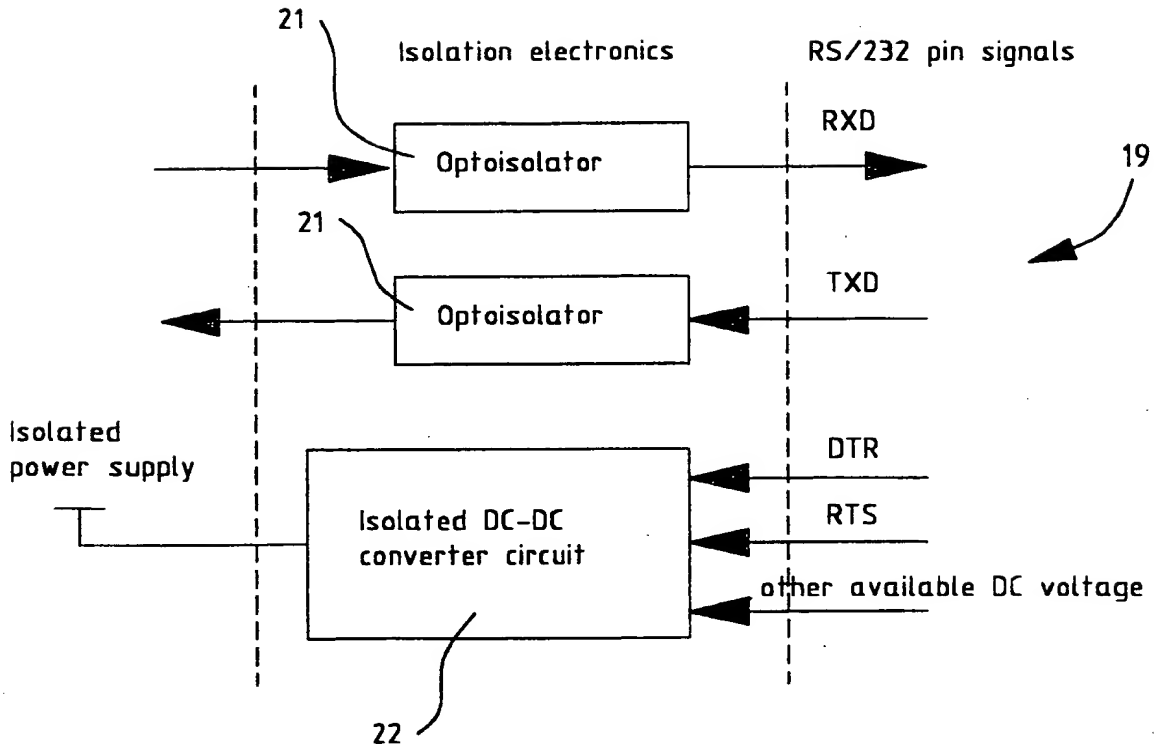


Fig. 3

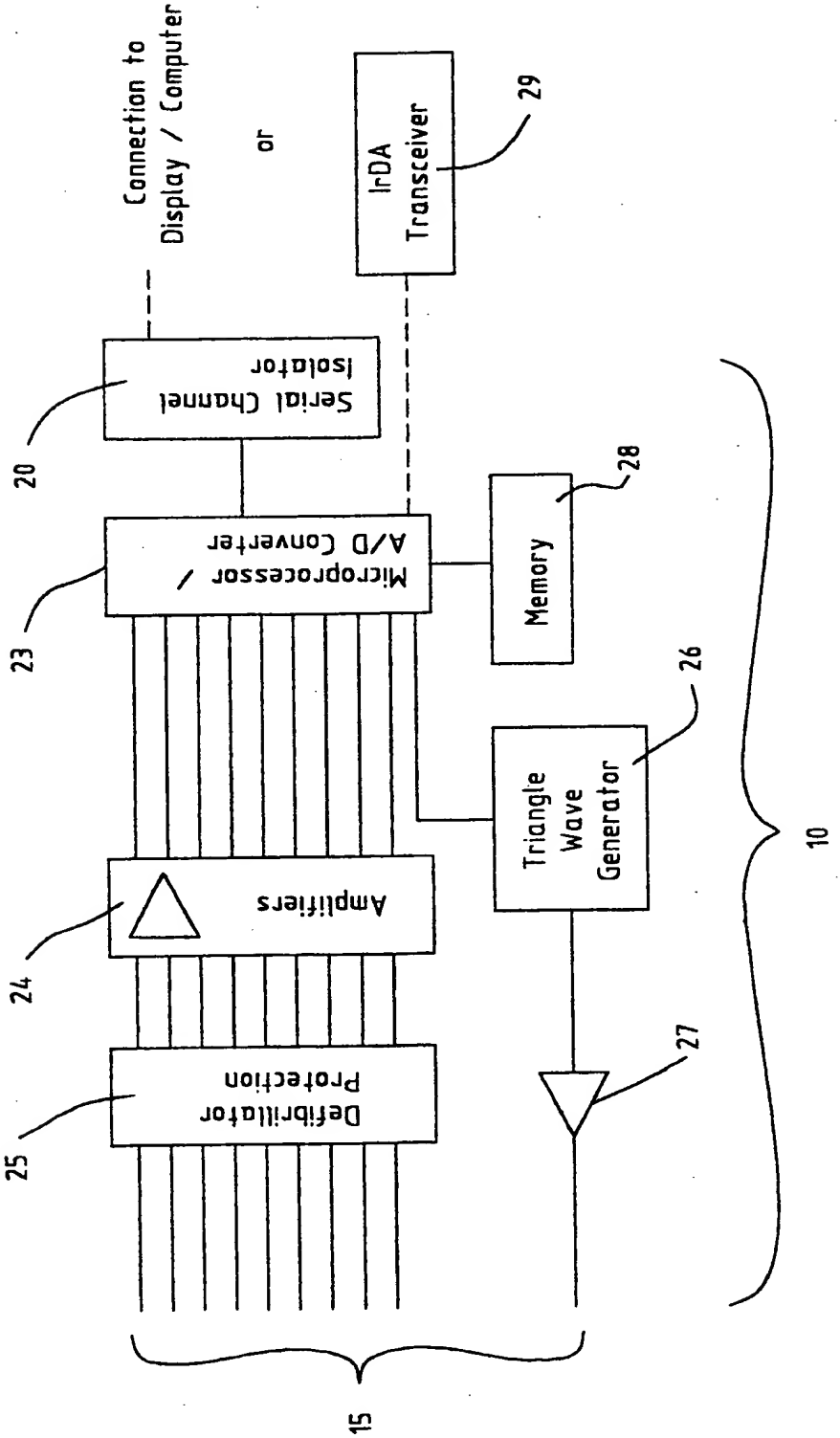


Fig. 4

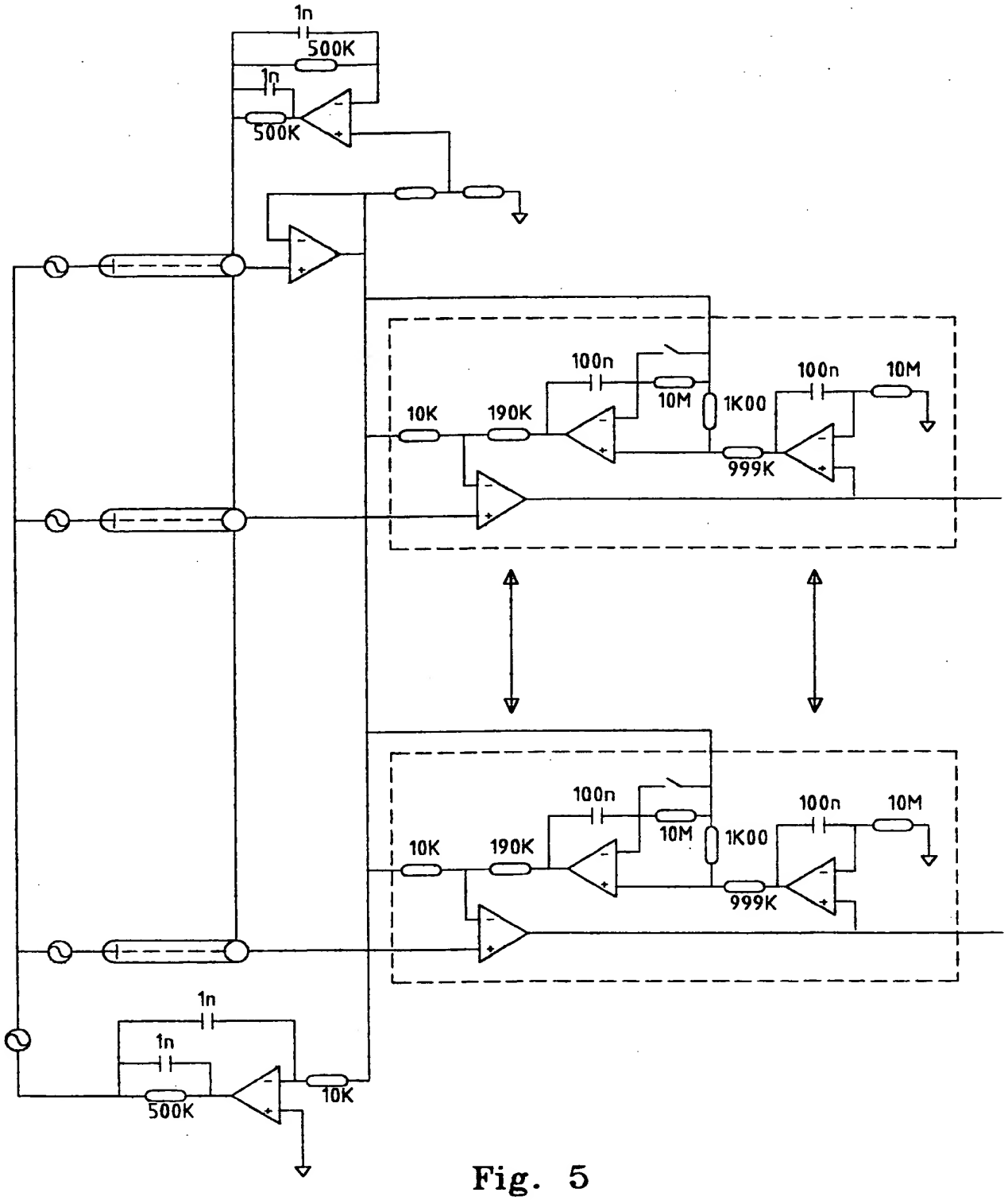
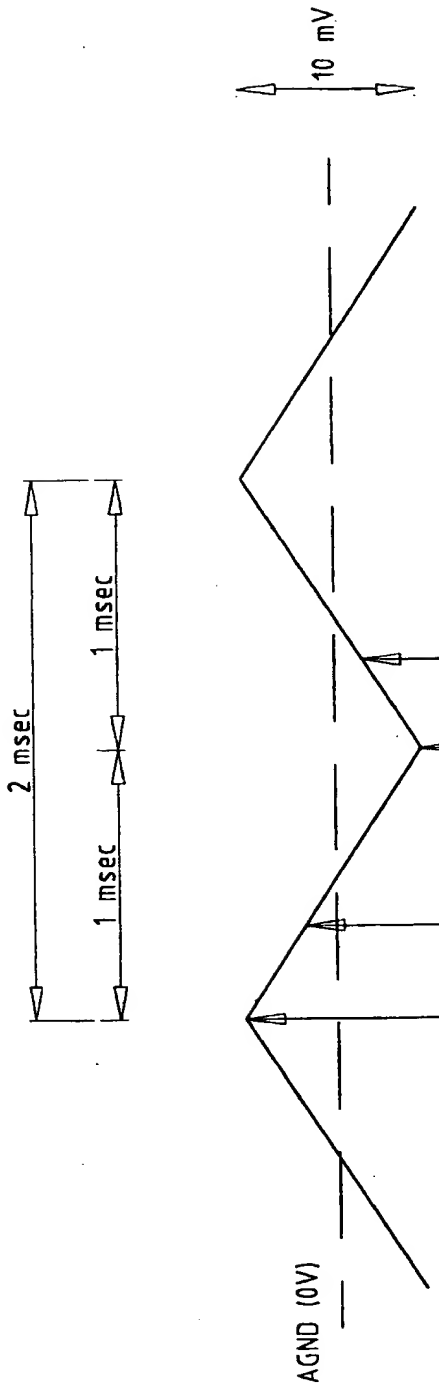


Fig. 5



$V_{samp\ i} = A_i + B_i$ gives sample voltages for 2msec period

$[A_i - B_i] <$ THRESHOLD normally

$>$ THRESHOLD → LEADS OFF

$[A_i - AGND] = -[B_i - AGND] \quad \forall\ i = [1..8]$ so cancels

Fig. 6

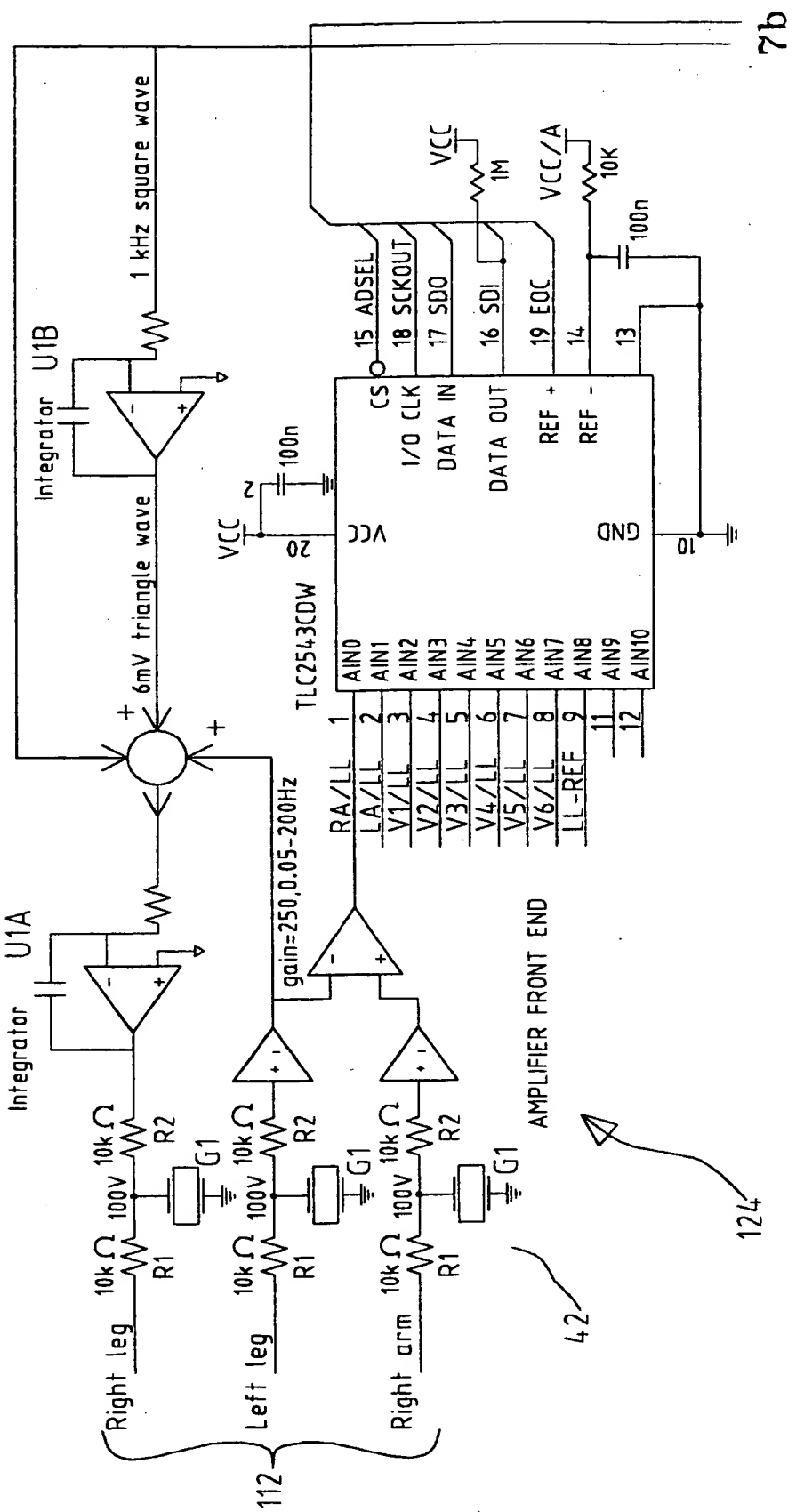


Fig. 7a

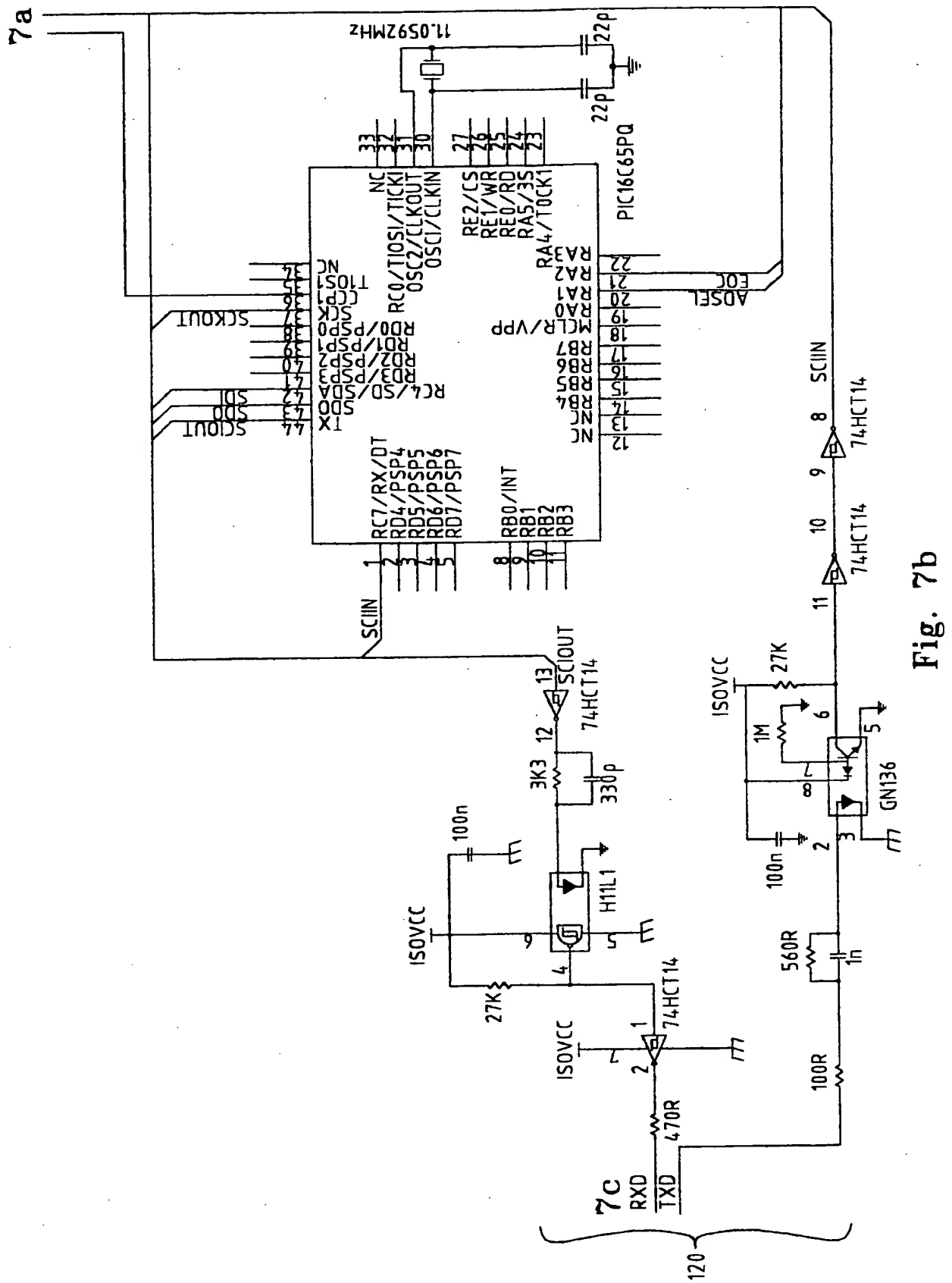


Fig. 7b

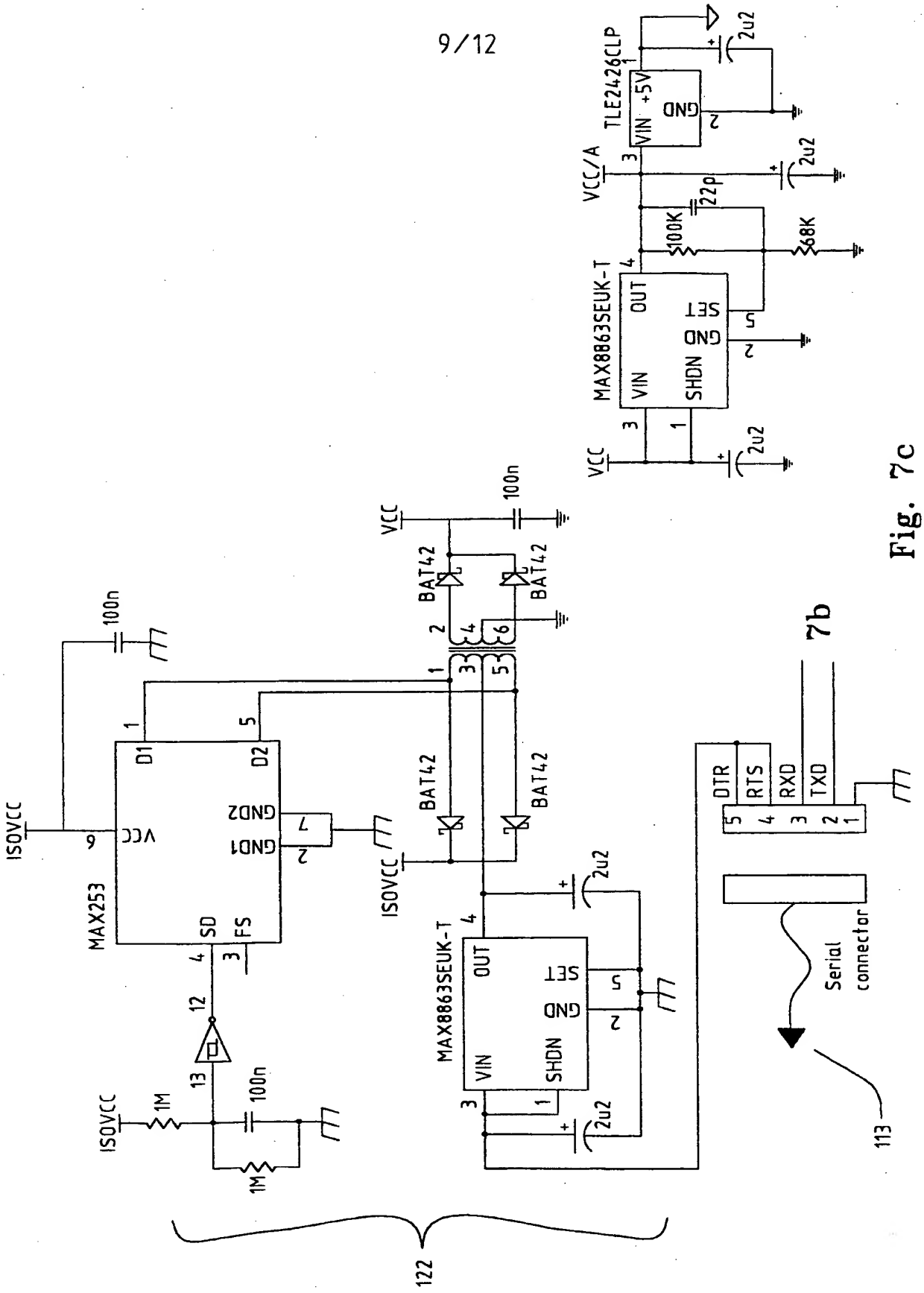


Fig. 7c

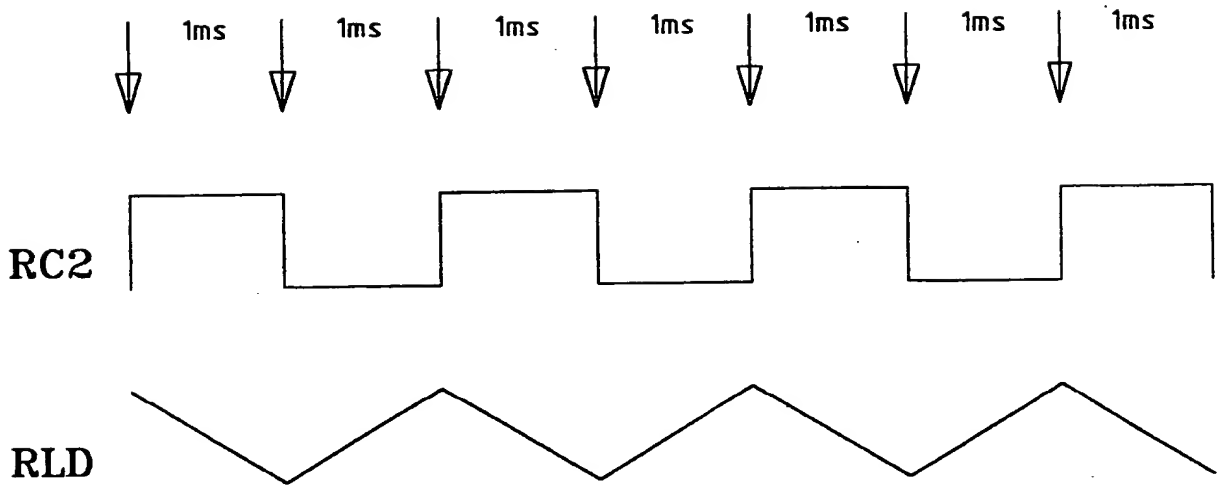
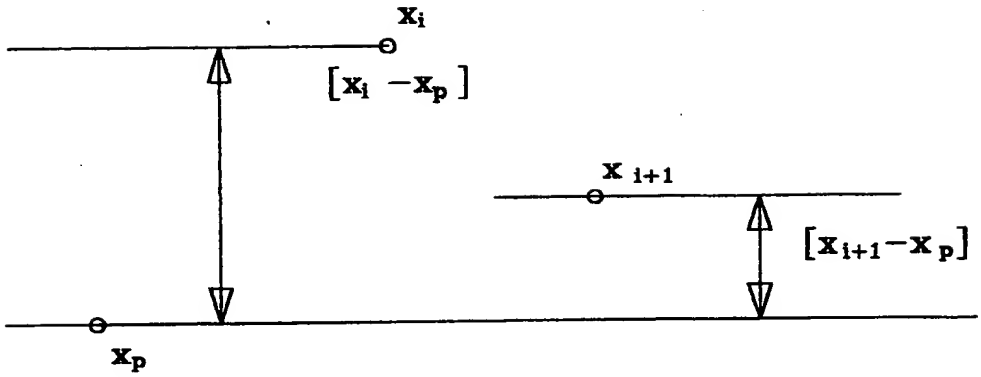


Fig. 8

COMMAND	PARAMETERS	DESCRIPTION	RESPONSE
enq		Inquire if a device is there	OK
id		Request device model, serial number, hardware and software revisions. Items are separated by semicolons.	(example) BIOSYNCH12;S12-1234;HWv1.0; SWv1.0
data		Start data transfer	OK then send packets until <ctrl> X is received, then enter command mode
ecg	all or any one of I,II.III,aVR,aVL,aVF, V1,V2,V3,V4,V5,V6	Request all ECG data (standard leads) ie. ecg all OR ecg I requests standard lead I power on default is lead II	OK does not commence data transfer until data command issued
sernum		Request 6 digit (numeric) device serial number	010000
res		Request resolution of LSB in nV; number of bits sampled	2971;12
pacing	on off (default)	Enable/disable pacing detection	OK
		Unknown command type	ERROR- what?

Fig. 9



If $[x_i - x_p] > [x_{i+1} - x_p]$
Then select x_i
Else select x_{i+1}

Fig. 10

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 98/00014

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: A61B 5/0402

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
A61B 5/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT:- ECG, EKG, ELECTROCARDIOGRA:, SERIAL:, PARALLEL:, IRDA, RS:, SCSI, COMM:(W) PORT#, TRANSMIT:
JAPIO:- same as WPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4924875 A (CHAMOUN) 15 May 1990 Fig. 2; column 4 line 32- column 5 line 13	1-9, 11-20, 22, 24-25
X	WO 91/02484 A1 (BIOMETRAK CORPORATION) 7 March 1991 Fig. 2; page 12 line 29-page 15 line 14	1-9, 11-20, 22, 24-25

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 1998	05 FEB 1998
Name and mailing address of the ISA/AU AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION PO BOX 200 WODEN ACT 2606 AUSTRALIA Facsimile No.: (02) 6285 3929	Authorized officer **W. GUNAWARDANA** Telephone No.: (02) 6283

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 98/00014

C (Continuation) **DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2272770 A (BISHOP et al.) 25 May 1994 Fig 1; page 4 line 8-page 8 line 35	1-8, 11-19, 22, 24-25
X	DE 4329946 A1 (CSM COMPUTER-SYSTEME MEßTECHNIK GmbH) 16 March 1995 Figs 1-3; column 3 line 46-column 5 line 53	1-8, 12-19, 24-25
X	WO 89/02247 A1 (SANDERS) 23 March 1989 Figs 1 and 3; page 6 line 2-page 10 line 26	1-6, 12-17
A	EP 488410 A1 (TERUMO KABUSHIKI KAISHA) 3 June 1992 Figs 1-10; column 2 line 27-column 4 line 3.	

INTERNATIONAL SEARCH REPORT
Information on patent family members

International Application No.
PCT/AU 98/00014

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	4924875	US	5020540				
WO	91/02484	US	5020540	AU	52801/90	CA	2064791
		EP	489010	US	4924875		
WO	89/02247	AU	25302/88	CA	1326884	US	4858617
EP	488410	AU	88304/91	US	5284151	JP	5007560

END OF ANNEX